(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 February 2003 (06.02.2003)

PCT

(10) International Publication Number
WO 03/010837 A1

(51) International Patent Classification[7]: H01L 51/20, 27/00

(21) International Application Number: PCT/NL01/00577

(22) International Filing Date: 26 July 2001 (26.07.2001)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **TECHNISCHE UNIVERSITEIT DELFT** [NL/NL]; Julianalaan 134, NL-2628 BL Delft (NL).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **BACHTOLD, Adrian** [NL/NL]; c/o Technische Universiteit Delft, Julianalaan 134, NL-2628 BL Delft (NL). **DEKKER, Cees** [NL/NL]; c/o Technische Universiteit Delft, Julianalaan 134, NL-2628 BL Delft (NL).

(74) Agent: **VAN BREDA, Jacques**; Octrooibureau Los en Stigter B.V., Weteringschans 96, NL-1017 XS Amsterdam (NL).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

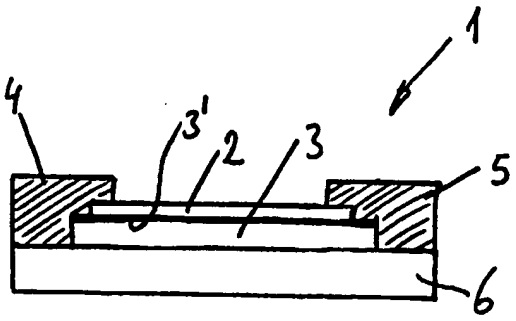
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: ELECTRONIC DEVICE USING CARBON NANOTUBES

(57) Abstract: Electronic device incorporating a tubular shaped carbon-molecule supported by a substrate, which molecule is provided with source and drain electrodes, and a gate electrode, wherein the gate electrode is a metallic electrode. The metallic electrode has a surface layer of oxide, preferably native oxide. The metallic electrode is selected from the group aluminium, zinc, copper.



WO 03/010837 A1

ELECTRONIC DEVICE USING CARBON NANOTUBES

The invention relates to an electronic device incorporating a tubular shaped carbonmolecule supported by a substrate, which molecule is provided with source and drain electrodes, and a gate electrode.

Such an electronic device is known from Nature, Volume 393, May 7, 1998, pages 15 to 17. From this publication a transistor is known having a so called semi-conducting carbon nanotube of about 1 nanometer in diameter that bridges source and drain electrodes. A gating voltage is applied to the silicon substrate that supports the carbon nanotube in order to induce carriers onto the nanotube to control the transistor.

When more than one or even many nanotube electronics are to be implemented on a silicon substrate the challenge then is to be able to control the respective transistors individually. It is therefore a prime objective of the invention to provide an electronic device according to the preamble of the main claim that is capable of being controlled individually.

A further objective is to provide such an electronic device having a gain of substantially more than one.

The electronic device according to the invention is therefore characterised in that the gate electrode is a metallic electrode. The metallic electrode in turn is preferably supported by the substrate.

Preferably the metallic electrode has a surface layer of oxide thus preventing short circuiting the source and drain electrodes. Native oxide provides an effective insulation layer with respect to both the carbon molecule per se and the respective source and drain electrodes. The oxide layer can also be grown for instance by evaporation, but should remain thin.

Particularly good results can be achieved when the metallic electrode is selected from the group consisting of aluminium, zinc and copper. Preferably however the metallic electrode is an aluminium electrode.

The invention will now be further elucidated with reference to the drawing.

In the drawing:

- fig. 1 shows a side view at the lay-out of an electronic device according to the invention;
- fig. 2 shows I-V characteristics of a single nanotube transistor according to the invention;
- fig. 3 shows several electronic devices according to the invention incorporating 1, 2 or 3 transistors.

Referring now first to fig. 1, a schematic device lay-out of an electronic device according to the invention is shown. The device 1 incorporates a tubular shaped carbon molecule 2 which is supported by an aluminium wire 3 which, at the side facing the tubular carbon molecule 2, is provided with an insulating native Al_2O_3 layer 3'. On both its extremities the tubular carbon molecule 2 is contacted by gold contacts 4 and 5 which are acting as the source and drain electrode respectively. The thickness of the Al_2O_3 layer 3' on the surface of the aluminium electrode 3 is in the order of magnitude of a few nanometers and much shorter than the separation between the contact electrodes 4 and 5 which is approximately 100 nanometer. This provides an excellent capacitive coupling between the gate electrode 3 and the tubular carbon molecule. This construction of the electronic device according to the invention allows for the integration of multiple similar devices acting as (nanotube) field effect transistors on the same substrate 6 whereby each transistor is individually controllable.

Fig. 2 shows the device characteristics of a typical nanotube FET. The variation of the current I through the device as a function of the gate voltage V_g (Fig. 2a) shows that very significant doping can be achieved. Starting with negative V_g, the current first decreases, then becomes immeasurably small, and finally increases again. This indicates that V_g shifts the Fermi level successively from the valence band (accumulation regime) to the gap (depletion) and finally to the conduction band (inversion) of the semi conducting nanotube. The nearby Al gate thus makes it possible to change the

doping of the nanotube over the full range from p-doping to n-doping. Several volts can be applied on the gate without destroying the oxide layer. This is quite remarkable since the insulator layer is only a few nanometers thin, and it indicates the excellent quality of the gate oxide. The breakdown threshold voltage where the layer is destroyed is typically between 2 and 5 V. A small gate leakage current (a few pA) is observed for V_g approaching such large gate voltages.

Fig. 2b shows the current versus bias voltage characteristics. Typical FET-type curves are found. For small source-drain voltages, the current changes rapidly then when the source-drain voltage V_{sd} is made more negative. This is called the linear regime because the current is proportional to V_{sd}. When V_{sd} becomes more negative than $V_g - V_t$, the current through the transistor changes more gradually (the saturation regime). Here V_t is called the threshold voltage at which (some) current starts to flow. It has a value of about -1.0 V for the transistor to which Fig. 2b relates. For a constant source-drain voltage in the saturation regime, the current has a parabolic dependence on the gate voltage $I \sim (V_g-V_t)^2$. This data shows that the transconductance of the nanotube transistors is 0.4μSiemens and the on/off ratio is at least 10^5. The maximum current that the nanotube transistor could tolerate was in the order of 100 nA and the on resistance was about R_{sd} = 33 MΩ for V_{sd}= -1.0 V, V_g = -1.3 V. Note that it is clear from Fig. 2a that even lower resistances can be achieved upon using higher gate voltages (80 kΩ for V_g = -3 V). A voltage gain of at least 10 can be achieved.

Fig. 3a shows the input-output characteristics of an inverter constructed from a nanotube transistor and an off-chip 100MΩ bias resistor. An inverter is a basic logic element that converts a logical 0 into a logical 1, and a logical 1 into a logical 0. When the input is a logical 1 (V_{in} = 0 V), then the nanotube is non conducting and the output is pulled to -1.5V, representing a logical 1.

The output voltage of an inverter should make a rapid transition from one logic level to the other as the gate voltage is swept. In this device according to the inven-

tion, the output voltage changes three times faster than the input voltage in the transition region indicating that this particular device has a voltage gain of 3 (other devices showed a gain of up to 6).

A NOR gate can be constructed by simply replacing the single transistor in the inverter with two transistors in parallel as shown in Fig. 3b. When either or both of the inputs are a logical 1 (V_{in} = -1.5 V), at least one of the nanotubes is conducting and the output is pulled to 0 V (logical 0). The output is a logical 1 only when both inputs are a logical 0 so that neither nanotube is conducting.

In Fig. 3b, the output voltage is plotted as a function of the four possible input states (0,0), (0,1), (1,0) and (1,1), verifying that this circuit indeed operates as a NOR gate. Using variations of the device circuitry one can realise any logical gate in this way.

A flip-flop memory element (SRAM) was constructed from two inverters, see Fig. 3c. When the output of each inverter is connected to the input of the other inverter, two different stable states are possible: The outputs can either take on the values (1,0) or (0,1). A logical 1 is written into memory by forcing the circuit into the (0,1) state and a logical 0 is written by forcing the circuit into the (1,0) state. To test the working of the memory cell, a voltage source was attached to one input and a logical 0 was written to V_{out} by driving V_{in} to -1.5 V. The switch was then opened again and the memory cell maintained a logical 1 at the output. These data thus demonstrate the stable memory function of a 2-transistor nanotube circuit according to the invention.

A 3-transistor device was realised in the ring oscillator shown in Fig. 3d. This circuit, used to generate an oscillating ac voltage signal, was built by connecting three inverters in a ring. A ring oscillator has no statically stable solution and the voltage at the output of each inverter consequently oscillates as a function of time. One of the inverter outputs is plotted in Fig. 3d. A clear voltage oscillation is observed. The 5 Hz frequency of the oscillations

is determined by the output impedance of the inverters (~1 GΩ) and the capacitance of the output nodes which currently is dominated by the ~100 pF parasitic capacitance of the wires connecting to the off-chip bias resistors.

A method to manufacture an electronic device according to the invention is explained below.

Al gates 3 for multiple nanotube transistors are first patterned using electron beam lithography on an oxidised Si wafer 6. During evaporation, the sample was cooled to liquid nitrogen temperature in order to minimise the roughness of the Al surface 3. The insulator layer 3' consists of the native oxide that grows by exposing the Al surface 3 to air. The precise thickness of this layer is in the order of a few nanometers. Carbon nanotubes 2 produced by laser ablation are dispersed on the wafer 6 from a dispersion in dichloroethane. Using an atomic force microscopy, those nanotubes 2 are selected that have a diameter of about 1 nm and that are situated on top of the Al gate wires 3. Their co-ordinates are registered with respect to alignment markers. Finally, contact electrodes 4,5 are fabricated with electron-beam lithography by evaporating Au directly on the nanotube 2 without adhesion layer.

CLAIMS

1. Electronic device incorporating a tubular shaped carbonmolecule supported by a substrate, which molecule is provided with source and drain electrodes, and a gate electrode, **characterised in that** the gate electrode is a metallic electrode.

2. Electronic device according to claim 1, **characterised in that** the metallic electrode has a surface layer of oxide, preferably native oxide.

3. Electronic device according to claim 1 or 2, **characterised in that** the metallic electrode is selected from the group aluminium, zinc, copper.

4. Electronic device according to claim 3, **characterised in that** the metallic electrode is an aluminium electrode.

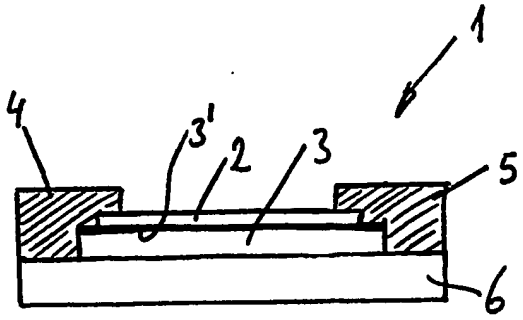


FIG. 1

fig. 2a

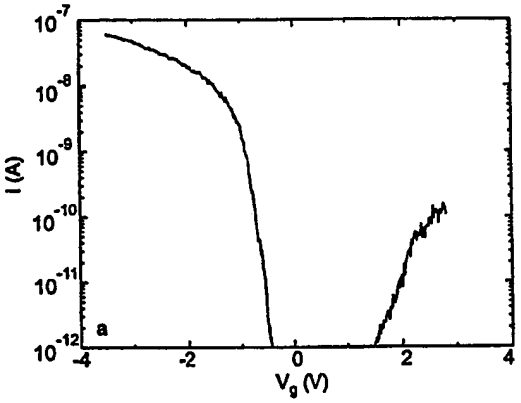
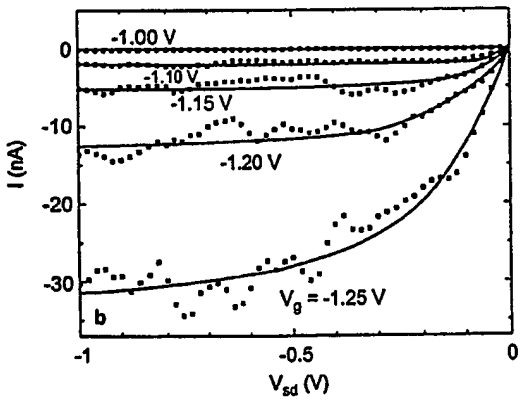

10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
I (A)
a
-4
-2
0
2
4
V_g (V)

fig. 2b


-1.00 V
-1.10 V
-1.15 V
-1.20 V
V_g = -1.25 V
0
-10
-20
-30
I (nA)
b
-1
-0.5
0
V_{sd} (V)

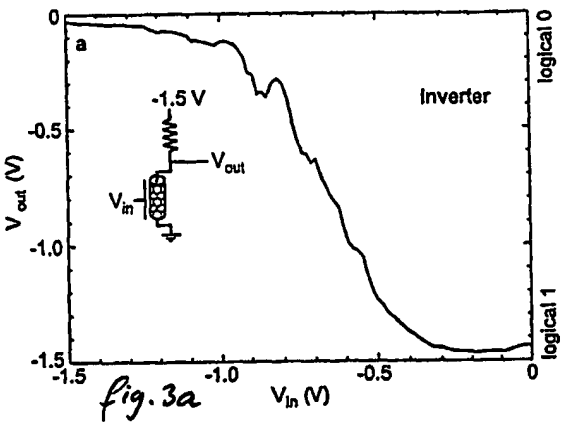


fig. 3a

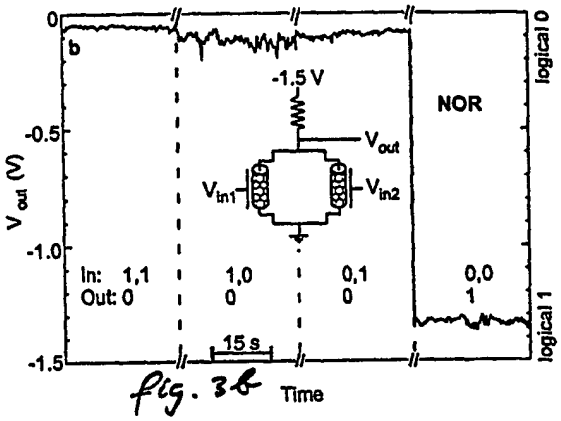


fig. 3b

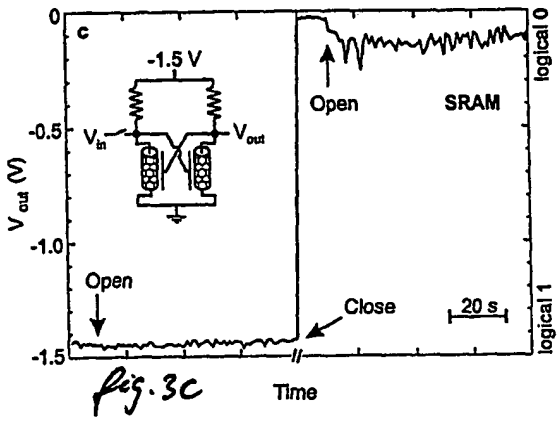


fig. 3c

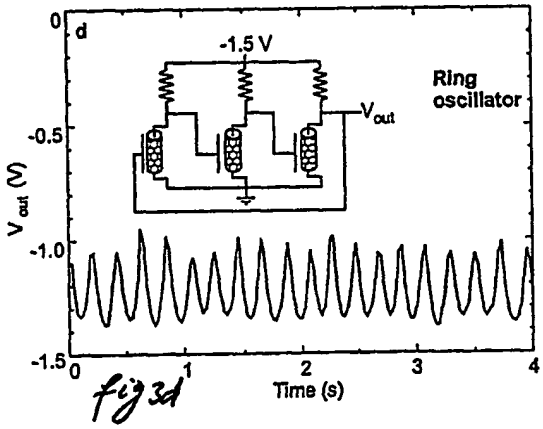


fig 3d

INTERNATIONAL SEARCH REPORT

PCT/NL 01/00577

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L51/20 H01L27/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
INSPEC, EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	MARTEL R ET AL: "SINGLE-AND MULTI-WALL CARBON NANOTUBE FIELD-EFFECT TRANSISTORS" APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 73, no. 17, 26 October 1998 (1998-10-26), pages 2447-2449, XP000996900 ISSN: 0003-6951 the whole document	1,3,4
Y	DE 44 01 442 C (SIEMENS AG) 23 March 1995 (1995-03-23) column 5, line 36 -column 6, line 17; figures 4,5	1,3,4

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 March 2002	08/04/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Königstein, C

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	RUECKES T ET AL: "CARBON NANOTUBE-BASED NONVOLATILE RANDOM ACCESS MEMORY FOR MOLECULAR COMPUTING" SCIENCE, AMERICAN ASSOCIATION FOR THE ADVANCEMENT OF SCIENCE,, US, vol. 289, no. 5476, July 2000 (2000-07), pages 94-97, XP000925696 ISSN: 0036-8075 the whole document	
A	YAMADA T: "ANALYSIS OF SUBMICRON CARBON NANOTUBE FIELD-EFFECT TRANSISTORS" APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 76, no. 5, 31 January 2000 (2000-01-31), pages 628-630, XP000934660 ISSN: 0003-6951 the whole document	
A	WO 00 51186 A (CLAWSON JOSEPH E JR) 31 August 2000 (2000-08-31) abstract; figures 2-4	

INTERNATIONAL SEARCH REPORT

Information on patent family members

PCT/NL 01/00577

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
DE 4401442	C	23-03-1995	DE	4401442 C1	23-03-1995
			DE	59508289 D1	15-06-2000
			EP	0664569 A1	26-07-1995
			JP	7240509 A	12-09-1995
			US	5540977 A	30-07-1996
WO 0051186	A	31-08-2000	EP	1159761 A1	05-12-2001
			WO	0051186 A1	31-08-2000